REMARKS

This communication is a full and timely response to the aforementioned final Office Action dated September 17, 2008. By this communication, claims 1 and 14-17 are amended. Claims 2-13 and 18-23 are not amended and remain in the application. Thus, claims 1-23 are pending in the application. Claims 1 and 14-17 are independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Rejections Under 35 U.S.C. § 102

Claims 1, 2, 5 and 12-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Takeshi Nagahori et al. ("An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection," IEEE Journal of Solid-State Circuits, Vol. 36, No. 12, pp. 1984-1991, December 2001, hereinafter "Takeshi").

Applicants respectfully submit that the applied references do not disclose or suggest all the recited features of the claimed invention for at least the following reasons.

With reference to Figure 1, for example, an exemplary embodiment of the present invention provides an optical semiconductor device that comprises an optical semiconductor element (e.g., laser diode (LD) 20) having a first electrode (e.g., cathode of LD 20), and a second electrode (e.g., anode of LD 20). The optical semiconductor device also comprises a a first conductor line connected to the first electrode (e.g., cathode of LD 20) of the optical semiconductor element (e.g., LD 20), and supplying a first electric signal (e.g., positive phase signal) to the optical semiconductor element (e.g., LD 20). The optical semiconductor device also comprises a second condutctor line connected to the second electrode (e.g., anode of LD 20) of the optical semiconductor element (e.g., LD 20), and supplying a second electric signal (e.g., anti-phase signal) to the optical semiconductor element (e.g., LD 20).

The optical semiconductor device of the exemplary embodiment also comprises a first inductance element (e.g., solenoid 21a) connected to the first electrode (e.g., cathode of LD 20) of the optical semiconductor element (e.g., LD 20) and the first conductor line. In addition, the exemplary optical semiconductor device comprises a second inductance element (e.g., solenoid 21b) connected between the second electrode (e.g., anode of LD 20) of the optical semiconductor element (e.g., LD 20) and a ground potential (e.g., the ground potential above the upper horizontal dotted line denoting LD module 2) such that one end of the second inductance element (e.g., solenoid 21b) is connected at the ground potential, and connected to the second conductor line.

The disclosed embodiment provides that the first and second conductor lines constitute a pair of differential lines. In addition, with reference to line 2 on page 20 to line 18 on page 21 of the specification, the exemplary embodiment provides that the first and second inductance elements (e.g., solenoids 21a, 21b) are configured to permit a bias current (e.g., from the ground potential to negative power supply Vee through LD module 2) to pass therethrough, and simultaneously prevent the first and second electric signals from passing therethrough, respectively.

As described in the paragraph beginning at line 2 on page 20, the solenoids 21a and 21b can be constituted, for example, by air-cored coils which cause bias currents (direct currents (DC)) to pass through, and which suppress modulated signals (electric signals) output from the LD driving circuit 1 from leaking from the first and second bias circuits 28a and 28b. In other words, the solenoids 21a and 21b respectively cut off the first and second electric signals and thereby prevent the first and second electric signals (modulated signals) from leaking, because the solenoids 21a and 21b respectively prevent the first and second electric signals from passing therethrough.

In addition, with reference to Figure 1, for example, the exemplary embodiment provides that the second inductance element (e.g., solenoid 21b) is connected between the second electrode (e.g., anode of LD 20) of the optical semiconductor element (e.g., LD 20) and a ground potential such that one end of the second inductance element (e.g., solenoid 21b) is connected at the ground potential. For instance, as shown in Figure 1, for example, one end of the second inductance

element (e.g., solenoid 21b) is connected to a ground potential and is therefore connected at the ground potential.

Independent claims 1 and 14-17 recite various features of the above-described exemplary embodiment.

In the Amendment filed on May 28, 2008, claims 1 and 14, 15 and 17 were each amended to recite that the second inductance element is connected between the second electrode of the optical semiconductor element and a ground potential. A similar amendment was made to claim 16 to define the structural arrangement of the second bias circuit. Applicants maintain that Takeshi does not disclose or suggest these configurations.

On the contrary, with reference to Figure 4 on page 1986, Takeshi discloses a laser diode driving stage (LDDRV) circuit having two connection lines to an LD (laser diode) chip carrier and parasitic elements of the LD. A first connection line is connected to a transistor Q3, an inductor (upper inductor), and to the anode of the LD through a resistor. A second connection line is connected to transistors Q2 and Q4, an inductor (lower inductor), and to the cathode of the LD. A second connection line is connected to a transistor Q3, an inductor (upper inductor), and to the anode of the LD through a resistor. The Office asserted that the aforementioned first connection line of Takeshi corresponds to the first conductor line of claim 1, and that the aforementioned second connection line of Takeshi corresponds to the second conductor line of claim 1. Accordingly, with reference to Figure 4, the Office apparently considers the upper inductor of Takeshi as corresponding to the first inductance element of claim 1, and considers the lower inductor of Takeshi as corresponding to the second inductance element of claim 1.

However, in contrast to claim 1, Takeshi does not disclose or suggest that the lower inductor is connected between the cathode of the LD and a ground potential. Even if the Office considers the lower inductor of Takeshi as being connected to a ground potential as illustrated in the LD chip carrier, the lower inductor is not connected between the cathode of the LD and the ground potential of the LD chip carrier. Similarly, the upper inductor of Takeshi is also not connected between the anode of the LD and a ground potential.

Despite the contradictory disclosure of Takeshi to the features of the claimed invention, the Office asserted that the phrase "connected between" does not specify a direct connection, but only that the specified element is somewhere on a path connecting the two end points.

To obviate this unduly broad interpretation, claims 1 and 14, 15 and 17 have each been amended to emphasize that the second inductance element is connected between the second electrode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential.

Claim 16 has been amended to recite that the second bias circuit is connected between the second electrode of the optical semiconductor element and a ground potential such that one end of the second bias circuit is connected at the ground potential.

Takeshi does not disclose or suggest this configuration. In contrast to claims 1 and 14-17, no end of the lower inductor of Takeshi is connected at the ground potential. On the contrary, the upper and lower inductors of Takeshi are respectively connected in series to the capacitors shown in the lower part of the LD Chip Carrier, and therefore are not connected at the ground potential shown in the LD Chip Carrier

Therefore, Applicants respectfully submit that Takeshi does not disclose or suggest a second inductance element connected between the second electrode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential, as recited in claims 1 and 14-17.

Furthermore, claims 1 and 14-17 each recite another distinguishing feature over Takeshi.

In particular, claims 1, 14, 15 and 17 each recite that the first and second inductance elements are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second electric signals from passing therethrough, respectively.

Claim 16 recites that the the first and second bias circuits are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second differential signals from passing therethrough, respectively.

On the contrary, the upper and lower inductors of Takeshi pass the signals modulated at transistors Q1 and Q2 to the laser diode LD. This is a necessary operation for the function of the laser diode LD of Takeshi.

Therefore, Applicants respectfully submit that Takeshi does not disclose or suggest that the upper and lower inductors permit a bias current to pass therethrough, and simultaneously prevent (1) first and second electric signals or (2) first and second differential signals therethrough, as recited in claims 1 and 14-17.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claims 1 and 14-17 are patentable over Takeshi, since Takeshi does not disclose or suggest all the recited features of claims 1 and 14-17.

Dependent claims 2-13 and 19-23 recite further distinguishing features over Takeshi.

II. Rejections Under 35 U.S.C. § 103(a)

Dependent claims 3, 4 and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeshi in view of Ciubotaru et al. (U.S. 2003/0086455, hereinafter "Ciubotaru"). Dependent claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeshi in view of Ito et al. (U.S. 4,975,664, hereinafter "Ito"). Dependent claims 7-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeshi in view of Ito and further in view of Kobayashi et al. (U.S. 5,982,793, hereinafter "Kobayashi").

As demonstrated above, Takeshi does not disclose or suggest a second inductance element or second bias circuit connected between the second electrode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential, as recited in claims 1 and 14-17. Furthermore, Takeshi does not disclose or suggest first and second inductors or first and second bias circuits which are configured to permit a bias current to pass therethrough, and simultaneously prevent first and second electric signals or first and second differential signals from passing therethrough, as recited in claims 1 and 14-17.

Similar to Takeshi, Ciubotaru, Ito and Kobayashi fail to disclose or suggest the features of the first and second inductance elements as recited in claims 1 and 14,

15 and 17, and fail to disclose or suggest the features of the first and second bias circuits as recited in claims 16.

Therefore, no combination of Takeshi, Cibotaru, Ito and Kobayashi would result in the subject matter of claims 1 and 14-17, since these references, either individually or in combination, fail to disclose or suggest all the recited features of claims 1 and 14-17.

Having sufficiently described the patentability of independent claims 1 and 14-17 for at least the reasons presented above, Applicants respectfully submit that it is unnecessary at this time to separately discuss the additional patentable features of the dependent claims, and address the Office's interpretation of the references applied against the dependent claims. However, Applicants reserve the right to do so if it becomes appropriate.

III. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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